IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hiroaki Niimi, et al. **Art Unit: 2823**

Serial No.: 09/885,744 **Examiner: Khiem D. Nguyen**

Filed: 06/20/01 **Docket: TI-32705**

For: METHOD FOR ANNEALING ULTRA-THIN, HIGH QUALITY GATE OXIDE LAYERS USING OXIDIZER/HYDROGEN MIXTURES

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Karen Vertz 2-16-04
Karen Vertz Date

Transmitted herewith in triplicate is an Appeal Brief in the above-identified application. The Commissioner is hereby authorized to charge the ***$330.00*** fee for this appeal, or credit any overpayment to Account No. 20-0668. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Niimi et al	Art Unit 2823
Serial No:	09/885,744	Examiner Nguyen
Filed:	06/20/2001	Docket TI-32705

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Commissioner for Patents
P.O. Box 1450
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BRIEF ON APPEAL

Sir:

This is an Appeal from the Final Rejection mailed 08/19/2003.

The Real Party in Interest is Texas Instruments Incorporated, assignee of record.

There are no related appeals or interferences.

Status of Claims

Claims on Appeal are 1-7 and 9-13. Claims 14-16 are withdrawn from consideration.

Claim 8 was canceled.

Status of Amendments

All Amendments have been entered.

Summary of Invention

In the fabrication of microelectronic semiconductor circuits, the invention provides a method for forming an improved ultra-thin dielectric layer (0.6 to 2.0 nanometers thick). Typically, the dielectric layer is to be used for MOS transistor gate insulation.

First, an ultra-thin oxide layer is formed on the surface of a semiconductor substrate. Subsequently, the oxide layer is treated to add a uniform nitrogen distribution throughout the oxide layer. Subsequently, the nitrided layer is annealed and re-oxidized by exposure to a mixture of N2O and H2 at high temperatures. This step stabilizes the nitrogen distribution, heals plasma-induced damage, and reduces interfacial defect density.

Figures 1-3 and 11, and the corresponding portions of the specification, illustrate the process sequence of the claimed invention. Beginning at page 10, line 22, Fig 1 is described, showing the formation of oxide layer 103. Beginning at page 11, line 5, Fig 2 is described, showing the nitridation of oxide layer 103 to provide a uniform nitrogen distribution therein. Beginning at page 11, line 30, Fig 3 is described, showing the re-oxidation and annealing step. At the top of page 12, four alternate annealing steps are listed. Step 313 (Fig 11) is the only annealing step included within the claims on appeal.

Issues

The sole legal issue presented on appeal is whether or not the claimed subject matter is patentable over the cited prior art (35 USC 103).

There are factual issues regarding the Examiner's description of the Huang et al reference, U.S. Publication No. 2002/0146914 A1.

Grouping of Claims

Claims 1,3,4 and 7 should stand or fall together.

Claim 2 limits the process to the formation of an ultra-thin dielectric layer, and may therefore be considered patentably distinct from claims not so limited.

Claims 5 and 6 are limited to specific times, temperatures, and pressures for the anneal step, which are patentably distinct from the broader claims.

Claims 9-13 are limited to the fabrication of specific circuit structures, and are therefore patentably distinct from the broader claims.

Arguments

The rejection of claims 1-7 and 9-13 as unpatentable over Huang et al in view of Daniel et al and Park et al should be reversed, because the references do not disclose or suggest the subject matter of the invention, whether taken singly or in combination.

There are only two embodiments of the Huang et al process. One embodiment is illustrated by Fig 2; and the other by Fig 4. In the embodiment of Fig 2 there is **only one growth step,** and **no** annealing step. The growth step produces oxide and nitride at the same time. (Fig 3 is only an explanation of what already happened in Fig 2.) In paragraph [0021] of Huang et al there is a clear statement that oxynitride layer 104 has a **non-uniform** nitrogen content.

In the second embodiment of Huang et al (Fig 4) a silicon nitride layer is formed on the substrate, followed by the growth of oxynitride in the same manner as in the growth step of Fig 2. In Fig 5, the resulting dielectric layer is shown to have a nitrogen content in surface region A that is "much higher than region B". (See paragraph [0023].) Huang et

al explains that such non-uniformity is required, in order to "act as a barrier to inhibit boron penetration" from the gate (paragraphs [0021] and [0024]).

Applicants' process has three separate high-temperature steps: 1) oxide growth, 2) **uniform** nitridation of the oxide, and 3) annealing. Compared with the first embodiment of Huang et al, applicants have two extra steps, a different purpose, and a different result. Compared with the second embodiment of Huang et al, applicants' process has an opposite sequence (oxidation followed by nitridation) and a clear emphasis on a uniform nitrogen distribution, in sharp contrast to Huang's requirement of **non-uniform** nitrogen distribution.

Clearly, the Huang et al process is not the same as, and does not suggest the method claimed by applicants. The result is also not the same and not equivalent.

The secondary reliance upon Daniel et al to show uniform nitrogen distribution is not properly combined with Huang, because it **directly contradicts an essential feature** of Huang et al. The courts have repeatedly held that a secondary reference must not be combined in a manner "that would destroy the essence" of the primary reference.

Still further, the Examiner has combined Daniel et al with a **grossly inaccurate** version of Huang et al. The Final Rejection states that Huang et al discloses forming an oxide layer "and subsequently" reoxidizing the layer by a rapid anneal step. This description of Huang is simply wrong. Instead, the complete embodiment of Fig 2 in Huang et al is a single-step method for the growth of oxide and nitride **at the same time.** Huang does not start with an oxide layer; and there is no "subsequent" anneal step and no "subsequent" reoxidation step. (Fig 4 of Huang et al is even more remote, since it starts with a nitride layer.)

The Rejection further states that it would be "obvious" to modify the Huang et al process to obtain uniform nitrogen distribution, in view of Daniel et al. But the Examiner does not address the question of **how** to modify the Huang et al process in order to obtain the Daniel result. It cannot be obvious to ignore the express teachings of the primary reference, and to substitute a different step to obtain a different result that **contradicts** the desired result of the primary reference.

Still further, if indeed it were possible to obtain uniform nitrogen distribution in the Huang process, it would still be a **one-step growth** process to form oxide and nitride at the same time. But Huang et al expressly teaches that such a one-step process yields a **non-uniform** nitrogen distribution! How does one reconcile that with the Examiner's speculative assumption that the Daniel disclosure disproves the Huang disclosure?

In any event, the Examiner's proposed modification of the Huang process would still be **one-step** growth, with no subsequent anneal step. This does **not** suggest the **three-step** method claimed by applicants.

The Examiner further speculates that a modified one-step Huang method could yield applicants' result. The Examiner is not qualified to substitute his own opinion on such a question. However, in any event "the same result" is not a relevant issue. Even if we had proof that applicants' method yields a known result, it would not be relevant. The Examiner's premise seems to be that a novel method cannot be patentable if it yields a known result. The plain fact is that thousands of patents have been properly issued for inventive methods that yield a known product.

Park et al is relied upon to show a capacitor, and is therefore relevant to claim 13 only.

For all the above reasons, the rejection should be reversed.

Respectfully submitted,

Gary C. Honeycutt

Gary C. Honeycutt, Reg.No. 20,250
Attorney for Applicants
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Certificate of Mailing

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Gary C. Honeycutt

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2/16/04

APPENDIX

CLAIMS ON APPEAL

~~WE CLAIM~~:

1. A method for forming an integrated circuit structure, comprising the steps of:

providing a substrate having a semiconductor surface;

forming an oxygen-containing layer on said semiconductor surface; then subsequently

forming a uniform nitrogen distribution throughout said oxygen-containing layer; and subsequently

re-oxidizing said layer by a rapid anneal step in an oxidizer and hydrogen mixture of N2O and H2 for stabilizing the nitrogen distribution, healing plasma-induced damage, and reducing interfacial defect density.

2. The method according to Claim 1 wherein said oxygen-containing layer is an ultra-thin silicon dioxide layer in the thickness range from 0.6 to 2.0 nm.

3. The method according to Claim 1 wherein said oxygen-containing layer is an oxynitride layer.

4. The method according to Claim 1 wherein said step of forming an oxide is a rapid thermal oxidation.

5. The method according to Claim 1 wherein said anneal steps comprise 5 to 60 s at 800 to 1050 °C in N2O/H2, flowing at 1 to 20 standard liters/min at 2 to 50 Torr.

6. The method according to Claim 5 wherein said N2O/H2 mixture contains 0.5 to 30 % H2 with the balance N2O.

7. The method according to Claim 1 wherein said oxidizer and hydrogen mixture comprises NO and H2, or O2 and H2.

9. The method according to Claim 1 wherein said integrated

circuit structure includes a transistor having a conductive gate structure disposed on a gate dielectric layer;

wherein said dielectric layer, after annealing and re-oxidizing, forms said gate dielectric layer; and further comprising the step of:

forming said conductive gate structure upon said gate dielectric layer.

10. The method according to Claim 9 wherein said conductive gate is comprised of doped poly-silicon.

11. The method according to Claim 9 wherein said gate dielectric is an ultra-thin silicon dioxide layer.

12. The method according to Claim 9 further comprising the steps of forming source and drain and their respective contact to complete said transistor.

13. The method according to Claim 1 wherein said integrated circuit structure includes a capacitor having a capacitor dielectric; and further comprising the steps of:

forming a first electrode over said substrate, said semiconductor surface present at said first electrode; and

forming a second electrode on said dielectric layer; wherein said dielectric layer forms said capacitor dielectric.

~~14. An integrated circuit having a component as produced~~ by the ~~method~~ of Claim 1.

15. The circuit according to Claim ~~14~~ wherein said component is a ~~transistor~~.

16. The circuit ~~according to Claim 14 wherein~~ said ~~component is a capacitor.~~

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